Electroplating and Electroforming

Electrolytic and electroless plating on Si, SiC, GaAs, InP, GaN, glass, sapphire, and AlN ceramic: bump formation, UBM, void-free TSV and TGV copper fill, LIGA electroforming, and DPC on ceramic. The metal menu spans Cu, Ni, Au, Ag, Pd, Rh, Ru, Pt, AuSn, SnAg, and indium. From 1 wafer, managed end to end by a dedicated project manager.

300 mm
max wafer size; panels for TGV

1 µm
LIGA minimum structure diameter

Void-free
Cu TSV/TGV fill, SEM-verified

156°C
indium bumping melt point

Copper for vias: fill and conformal routes

01

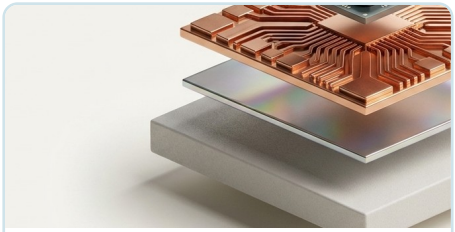
Void-free superfill

Bottom-up additive electrolyte chemistry fills TSV and TGV from the bottom, confirmed by cross-section SEM. Etch, liner, seed, and fill run as one project with DRIE, PECVD, and sputtering.

02

Conformal via plating

Cu or Ni on via sidewalls without fill: diffusion barrier, RF shielding sleeve, or coaxial feedthroughs for RF MEMS and mmWave packages. RF isolation is geometry-dependent and confirmed by test or simulation.



03

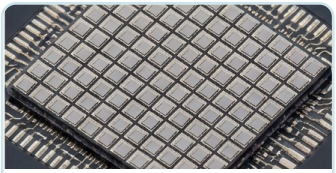
DPC on ceramic

Direct plating copper on AlN (170 W/m·K) and Al_2O_3 for IGBT, SiC MOSFET, and GaN power modules: a sputtered Ti/Cu adhesion layer makes the ceramic platable, then fine-pitch Cu is built up.

Bumps, UBM, and surface finishes

SnAg solder bumping

SnAg 96.5/3.5 for lead-free flip-chip; pitch from 100 µm, 20-100 µm bump height, post-plate reflow.

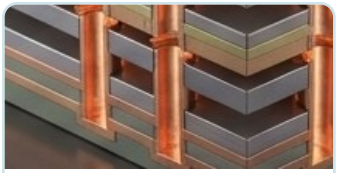


Indium bumping

156°C melt point for IR focal plane arrays (HgCdTe, InSb, InGaAs), cryogenic assemblies, and photonic co-packaging; Cu/Ni/In and Ni/In stacks.

ENIG / ENEPIG UBM

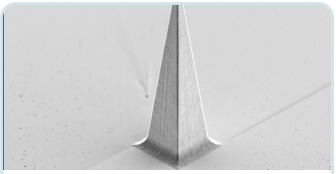
Electroless Ni/Au and Ni/Pd/Au for wafers that cannot accept external current: SiC and GaN power devices, fragile thin films, finished CMOS; wire-bondable, AEC-Q compatible.



Au, AuSn, and specialty finishes

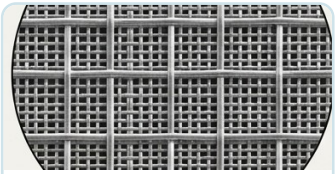
Au for wire- and ACF-bondable pads, AuSn 80/20 for hermetic photonics packages, Ag, Pd, Rh, Ru, and Pt where conductivity or chemical stability requires it.

LIGA electroforming and 3D microstructures



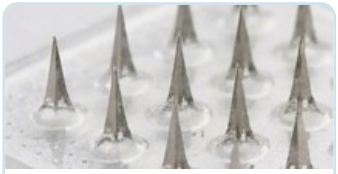
Ni, Pd-Ni, Ni-Co electroforming

X-ray LIGA resist molds electroformed into high-aspect-ratio metal structures with diameters from 1 µm; Pd-Ni and Ni-Co for hardness, wear resistance, and biocompatibility evaluation.



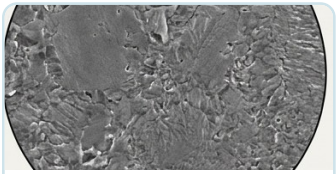
Micropore membranes

Nickel membranes with precise pore sizes from 1 µm for microfiltration, cell sorting, emulsification, and nebulizers.



Microneedle arrays

Hollow and solid Ni or Pd-Ni arrays for transdermal delivery and interstitial fluid sampling; biocompatibility characterized per program.



NIL molds

Nickel masters and working molds from Si or polymer originals; withstand thousands of imprint cycles for nanoimprint production.

Specifications (typical capability, confirmed per program)

Process	Key specification	Primary application
Cu TSV / TGV fill	Void-free superfill, SEM-verified; wafers to 300 mm, glass panels for TGV	3D-IC stacking, 2.5D interposers
Conformal Cu / Ni	Sidewall plating without fill	RF coaxial vias, shielding, barriers
LIGA electroforming	1 µm minimum diameter; Ni, Pd-Ni, Ni-Co	Microneedles, membranes, NIL molds
Indium bumping	156°C melt point; Cu/Ni/In, Ni/In stacks	IR detectors, cryogenic assembly
SnAg bumping	96.5/3.5; pitch from 100 µm; 20-100 µm height	Lead-free flip-chip
DPC on ceramic	AlN 170 W/m·K, Al_2O_3; Ti/Cu adhesion layer	SiC, GaN, IGBT power modules
ENIG / ENEPIG	Electroless, no external current; wire-bondable	Power device UBM, finished CMOS
Substrates	Si and SOI 4-12 inch (thin wafers to 60 µm), SiC, GaN-on-Si, GaAs, InP, glass, fused silica, sapphire, AlN, Al_2O_3, polyimide	Wafers, panels, and singulated chips

How to start

Send substrate, size, metal and thickness targets, pattern data or bump pitch, quantity, and target schedule. A process engineer reviews feasibility within 24 hours; a written quotation follows within 7-10 business days. Prototype plating on a single wafer verifies fill, stress, and finish before production lots.

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