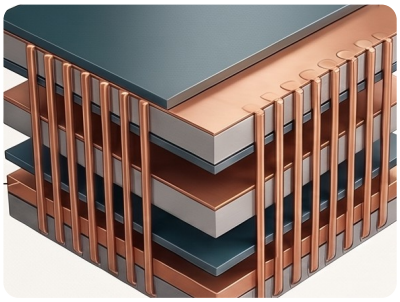
Through-Silicon Via (TSV) Fabrication

Five-step TSV flow from DRIE to CMP-ready Cu contacts, for 3D-IC memory stacking, 2.5D silicon interposers, and MEMS-on-CMOS integration. Every program is managed end to end by a dedicated project manager: one quotation, one process traveler, one point of contact. From 1 wafer.



>50:1
DRIE aspect ratio (depth:width)

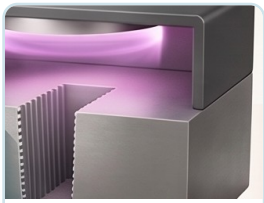
100 µm+
via depth, through-wafer or blind

Void-free
Cu fill, SEM-verified

2-12 in
wafer diameters

TSV: copper-filled vertical channels through the wafer connect stacked dies directly, shortening interconnects compared with wire bonds where the application and geometry allow. Illustrations in this brochure are schematic; the CMP panel shows the surface after bulk Cu removal, before final barrier clearance and inspection.

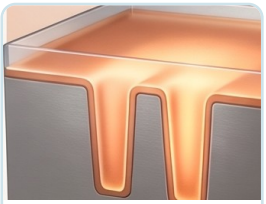
Process flow



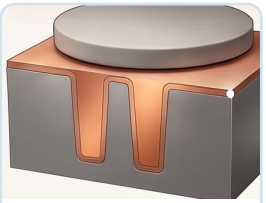
01
DRIE via etch
Bosch process (SF_6/C_4F_8), SiO_2 hard mask, selectivity above 100:1, sidewalls 89-90°, scallops below 100 nm.

02
Dielectric liner
PECVD SiO_2 (PE-TEOS) below 400°C for standard vias; ALD Al_2O_3 for near-conformal coverage in narrow, deep vias.

03
Barrier and seed
TiN, Ta, TiW, or Ti diffusion barrier; sputtered Cu seed with ionized or collimated PVD for deep vias.



04
Cu electroplating
Bottom-up superfill with additive chemistry; post-plate anneal at about 400°C in N_2 (via-last flows below 300°C).



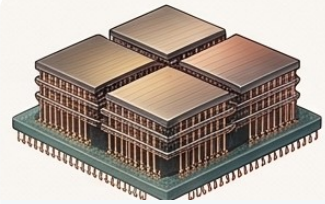
05
CMP
Bulk Cu overburden removal, then field barrier clearance where isolation requires it; endpoint and final topography (step height below 5 nm) confirmed for the stack.

Specifications (typical capability, confirmed per program at engineering review)

Parameter	Specification / range	Notes
Via etch method	DRIE, Bosch process	SF_6/C_4F_8 alternating cycles
Aspect ratio (depth:width)	>50:1	Depth above 100 µm, width from about 3 µm
Via depth	100 µm and deeper	Through-wafer or blind via
Hard mask	SiO_2	Si:SiO_2 selectivity above 100:1
Dielectric liner	PECVD SiO_2 (PE-TEOS); ALD Al_2O_3	Below 400°C; ALD for narrow vias
Diffusion barrier	TiN, Ta, TiW, Ti	Prevents Cu diffusion into Si and oxide
Cu seed	Sputtered PVD	Ionized or collimated PVD for deep vias
Cu fill	Electroplating, superfill	Void-free, confirmed by cross-section SEM

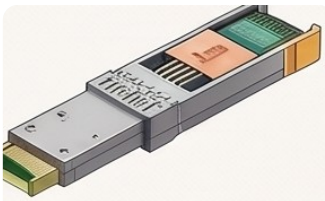
Parameter	Specification / range	Notes
Post-plate anneal	About 400°C, N_2 (route dependent)	Grain stabilization, stress relief
CMP endpoint	Eddy current or optical on the Cu overburden	Bulk Cu removal is followed by field-barrier clearance where required for electrical isolation; endpoint and final topography are confirmed for the stack
Post-CMP topography	Below 5 nm step height	Dishing and erosion measured
Wafer size	2 inch to 12 inch (300 mm)	All standard diameters
Integration timing	Via-first, via-middle, via-last	Via-first vias normally polysilicon or W filled; Cu for via-middle and via-last

Applications



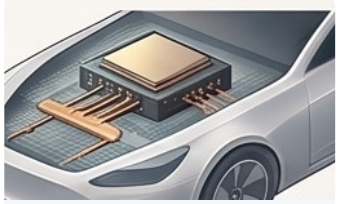
3D-IC memory stacking

Vertical die-to-die interconnect for HBM-class stacks; TSV, reveal, RDL, UBM, and C4 bumping in one project.



Silicon photonics packaging

TSV interposers for 800G/1.6T transceiver modules, with AuSn die attach and optical facet processing in the same project.



MEMS-on-CMOS and sensors

Backside contacts that remove bond-wire parasitics for high-bandwidth readout; hermetic-compatible flows.

Image sensors and 2.5D interposers

Backside-illuminated sensor readout and chiplet routing on silicon interposers for AI accelerators and HPC.

How to start

Send substrate, wafer size, via diameter and depth, quantity, and target schedule. A process engineer reviews feasibility within 24 hours; a written quotation follows within 7-10 business days. NDA available before any design file is shared. GDSII, DXF, and DWG accepted.

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