

TSV Fabrication Through-Silicon Vias for 3D Integration

The complete five-step TSV flow, DRIE etch to endpoint-controlled CMP, performed in the same coordinated project and managed end to end by a dedicated project manager.

Aspect ratio >50:1

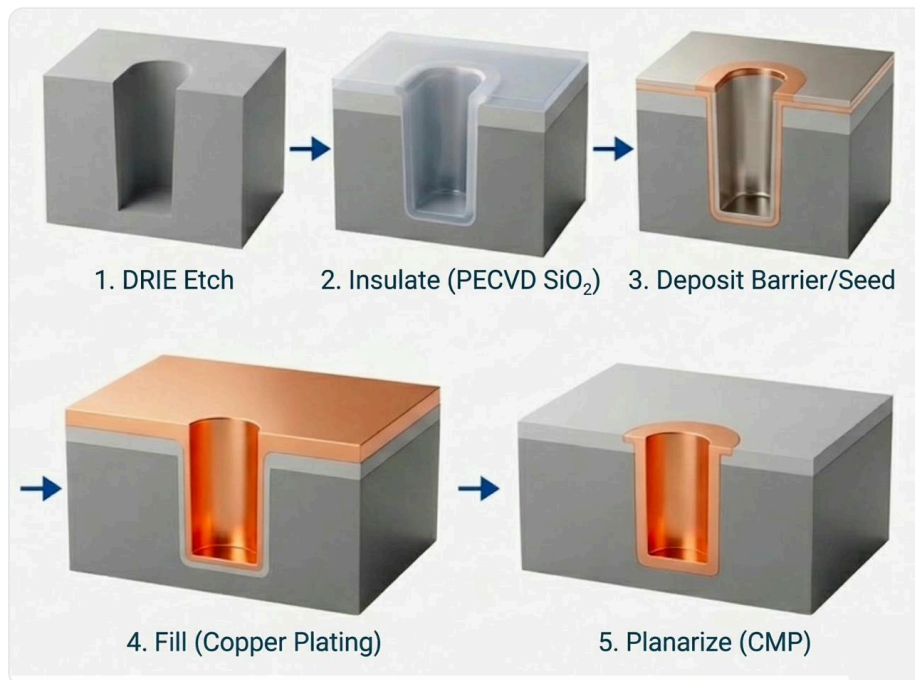
Depth >100µm

Void-free Cu fill

2 to 12 inch wafers

From 1 to 5 wafers · NDA from day one

01 The Five-Step TSV Process Flow



STEP 1

DRIE Etch

Bosch process, SF₆/C₄F₈ cycles. >50:1 aspect ratio, scallop <100nm, sidewall 89-90°.

STEP 2

Dielectric Liner

PECVD SiO₂ below 400°C. ALD Al₂O₃ option for near-100% step coverage.

STEP 3

Barrier & Seed

TiN, Ta, TiW, or Ti diffusion barrier. Sputtered Cu seed, ionized PVD for deep vias.

STEP 4

Cu Fill & Anneal

Bottom-up superfill electroplating, void-free by SEM. Anneal ~400°C in N₂.

STEP 5

Endpoint CMP

Eddy current or optical endpoint, stops on barrier. Topography <5nm.

02 Why Nanosystems JP Inc.

One coordinated project

All five steps quoted, scheduled, and reported as one project with a single point of contact. No re-quoting between steps.

All three integration timings

Via-first, via-middle, and via-last flows supported, matched to your device architecture and thermal budget.

Prototype-friendly

From 1 to 5 wafers with engineer-to-engineer communication and a feasibility answer within 24 hours.

03 Complete TSV Fabrication Specifications

| Parameter | Specification / Range | Notes |
|-----------------------------|------------------------------------|---|
| Via etch method | DRIE, Bosch process | SF ₆ /C ₄ F ₈ alternating cycles |
| Aspect ratio (depth:width) | >50:1 | Depth >100µm, width from ~3µm |
| Via depth | Up to >100µm | Through-wafer or blind via |
| Sidewall angle | 89-90°, near vertical | Bosch scallop <100nm amplitude |
| Hard mask | SiO ₂ | >100:1 selectivity over Si |
| Dielectric liner, standard | PECVD SiO ₂ (PE-TEOS) | High step coverage, <400°C |
| Dielectric liner, conformal | ALD Al ₂ O ₃ | Near-100% coverage for narrow vias |
| Diffusion barrier | TiN · Ta · TiW · Ti | Prevents Cu diffusion into Si/oxide |
| Cu seed layer | Sputter PVD | Ionized PVD / collimated for deep vias |
| Cu fill method | Electroplating, superfill | Bottom-up fill, additive chemistry |
| Fill quality | Void-free | Confirmed by cross-section SEM |
| Post-plate anneal | ~400°C, N ₂ atmosphere | Grain stabilization, stress relief |
| CMP endpoint | Eddy current / optical | Stops on barrier layer |
| Post-CMP topography | <5nm step height | Dishing and erosion measured |
| Wafer size | 2 inch to 12 inch (300mm) | All standard wafer diameters |
| Via integration timing | Via-first · middle · last | Process flow dependent |

04 Via Integration Timing

| | | |
|---|--|--|
| <p>1. Via-First</p> <p>TSV etched and filled before the CMOS front end. Highest via density, smallest pitch, high-temperature anneal allowed.</p> <p>Highest density · min pitch</p> | <p>2. Via-Middle</p> <p>Formed after transistors, before BEOL metal. The most common approach, widely used for memory and mixed-signal devices.</p> <p>Most common · <400°C anneal</p> | <p>3. Via-Last</p> <p>Etched and filled after all BEOL metal. Maximum design flexibility, ideal for interposers and MEMS + CMOS stacking.</p> <p>Interposer · MEMS+CMOS · <300°C</p> |
|---|--|--|

05 Where TSV Is Used Today

| | |
|--|---|
| <p>3D 3D-IC HBM Memory Stacking</p> <p>Thousands of fine-pitch TSVs connect stacked DRAM to the logic die in HBM2/HBM3 for AI accelerators.</p> | <p>2.5D 2.5D Silicon Interposer</p> <p>TSV arrays route CPU, HBM, and I/O chiplets to C4 bumps at far finer pitch than organic substrates.</p> |
| <p>MEMS MEMS-on-CMOS Integration</p> <p>Bond-wire-free vertical routing for IMUs in drones, AR/VR headsets, and autonomous vehicles.</p> | <p>PIC Silicon Photonics Interposer</p> <p>Electrical feedthrough between EIC, PIC, and package substrate for co-packaged optics.</p> |

Start your TSV project

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